	L #	Hits	Search Text	DBs	Time Stamp
1	L1	14731	MIM or "metal-insulator-metal" or metal-insulator-metal	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/25 13:39
2	L2	2509	1 near4 capacitor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/25 13:51
3	L3	718	2 and (copper or Cu or "copper alloy")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/25 13:52

	L #	Hits	Search Text	DBs	Time Stamp
4	L4	120	3 and ((@ad<"20010104") or (@rlad<"2010104"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/25 15:06
5	L5	405322	SiN or "silicon nitride"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/25 15:07
6	L6	65	4 and 5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/25 15:07

DOCUMENT-IDENTIFIER: US 20020113297 A1

TITLE: Method and structure of a precision mim fusible circuit
elements using fuses and antifuses

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Application Filing Date - APD (1):
20000314

Summary of Invention Paragraph - BSTX (6):
[0005] Integrated circuit **capacitors are formed as metal-insulator-metal capacitors (MIM** caps). "Back end of line" (BEOL) refers to the fabrication of the integrated circuit that occurs after the after the die contacts have been attached. BEOL MIM caps have replaced the very large area silicon capacitors in an effort to save silicon wafer area. However, the MIM caps are not as close to the external package as desired. The closer the precision capacitor to the external package, the better the effectiveness of the **MIM capacitor**. Another reason the **MIM caps are not precision capacitors** is due to the high variability in thickness of the deposited insulator (dielectric).

Summary of Invention Paragraph - BSTX (7):
[0006] **MIM capacitors** are used on RF receiver circuits. **MIM capacitors** are sensitive to electrical overstress (EOS) and electrostatic discharge (ESD) events. **MIM capacitors** fail at human body model (HBM) ESD events of 100 to 300 Volts. The need to isolate the failing section of the **MIM capacitor** or eliminate the fail mechanism is important for circuit reliability and yield.

Brief Description of Drawings Paragraph - DRTX (10):
[0020] FIG. 8 is a pictorial cross-sectional view of an alternative method of creating a capacitor where both plates are **copper**; and

Detail Description Paragraph - DETX (14):

[0034] The fusible link structure preferably is formed concurrently with the capacitor structure, where, in this case, the capacitor structure consists of a **copper** electrode, a trough, a deposited dielectric, the liner film and then a second **copper** electrode. The method of construction can be a Damascene process as shown in FIGS. 6A through 6C. In an illustrative example of this process shown in FIG. 6A, a first insulator film referred to as an interlevel dielectric, ILD1, (602) is formed on a silicon substrate (604). A second interlevel dielectric, ILD2, (606) is deposited upon ILD1 (602). Multiple interlevel dielectrics can be deposited in order to create multiple insulated levels of microcircuitry. A reactive ion etch (RIE) creates troughs (608) and (610) in ILD2 (606) which will ultimately form a **copper** connector and a fuse in this example. A first refractory liner (612) is deposited over the exposed surfaces. A **copper** deposition (614) is applied to fill the troughs (608) and (610).

Detail Description Paragraph - DETX (15):

[0035] A polishing operation removes the excess **copper** so that only the troughs (608) and (610) are filled with **copper** as shown in FIG. 6B. The **copper** forms conductive troughs (616) and (620). A mask, not shown, is used to allow removal of a portion of **copper** from the trough (620). The open portion of the trough (620) forms a fuse by having only the liner (612) available to carry the current input through conductor (618). This fuse can be blown in two ways: first excessive current in the trough (618) will cause overheating over the liner (622) and the liner will open circuit, secondly a laser can be directed at the bare liner to cause to fuse to open. Alternatively, the **copper** could be left in the fuse 620 and a laser could be directed at the fuse 620 to cause the fuse to open.

Detail Description Paragraph - DETX (16):

[0036] One method of forming a capacitor is shown in FIGS. 7A-7B. The trough (708) is etched into ILD2 (706) and overlayed with liner (712). Liner (712) is overlayed with an insulator (718). A second liner (722) is deposited on the insulator (718). A **copper** deposition (720) fills the remainder of trough (708). A polishing operation removes the excess **copper** to create a capacitor, shown in FIG. 7B, consisting of one plate (724) separated from a second plate (726) by a dielectric (728).

Detail Description Paragraph - DETX (17):

[0037] An alternative method of forming a capacitor is shown in FIG. 8. The trough (808) is etched into an ILD2 (806) and overlayed with a refractory liner (812). A **copper** deposition fills the trough and is polished as herein above described to create a first **copper** plate (824). A second liner of refractory metal (826) is deposited to overlay the first **copper** plate (824). An oxide dielectric (828) is deposited on top of the second liner (826). A third liner (830) overlays the oxide dielectric (828). An additional ILD3 (832) overlays the first **copper** plate (824), second liner (826), oxide dielectric (828), and third liner (830). In a similar manner a trough (834) is etched into ILD3 (832) to expose third liner (830). A fourth liner (836) overlays the trough (834). **Copper** is deposited on top of the fourth liner (836), and the excess polished off to create a second **copper** plate (838). A capacitor is thereby formed of second **copper** plate (838), dielectric (828), and first **copper** plate (824).

Detail Description Paragraph - DETX (18):

[0038] A double Damascene process can also be used. In this method two troughs are etched as shown in illustrative FIG. 9A-9B wherein a conductor

(924) on one ILD is connected to a second conductor (938) on another ILD by a via conductor (934). The via between microcircuit levels may be a **copper** interconnect, a resistive or capacitive element, or other circuit element to connect the different levels. In FIG. 9A a first etch creates a trough (908) in ILD2 (902). A first liner (912) is deposited in the trough (908). A **copper** deposition fills the remainder of the trough (908) and the excess **copper** and first liner (912) are polished off to create a first conductor (924). ILD2 (906) is deposited to overlay the circuitry if ILD1 (906). A second etch begins a double Damascene process by etching a second trough (930) deep enough to expose the first conductor (924). A second liner overlays the second trough (930) and the second trough is filled with **copper** (934), in this illustrative example. The excess **copper** and liner are polished off and a third etch creates the third trough (940) as shown in FIG. 9B. A third liner (936) overlays the third trough (940) and a **copper** deposition fills the third trough. A third polishing operation created the second conductor (938). A conductive link between two ILD has been created by the double Damascene process that created two troughs (930) and (940).

Claims Text - CLTX (21):

20. A method of forming a capacitor comprising: depositing a first insulator film; etching a first trough; depositing a first liner within said first trough; depositing a first conductive electrode within said trough; polishing off excess material; depositing a second insulator film over said first conductive electrode; etching a second trough extending through said second insulator film extending to said first **copper** electrode; cleaning surfaces; applying a thin dielectric over said exposed first **copper** electrode; depositing a second liner; depositing a second **copper** electrode;

and
polishing off excess material.